What is claimed is:

1. A semiconductor structure comprising a high-k material metal gate structure and a semiconductor gate structure,

wherein said high-k material metal gate structure includes:

a high dielectric constant (high-k) material portion having a dielectric constant greater than 8.0 and located on a semiconductor substrate;

a metal gate portion comprising a metal and vertically abutting said high-k material portion; and

an oxygen-impermeable dielectric spacer laterally abutting sidewalls of said high-k material portion and said metal gate portion;

and wherein said semiconductor gate structure includes:

a semiconductor oxide containing gate dielectric portion having a dielectric constant less than 8.0 and located directly on said semiconductor substrate;

a doped semiconductor portion comprising a doped semiconductor material and vertically abutting said gate dielectric; and

a low-k gate spacer comprising a dielectric material having a dielectric constant less than 4.0 and laterally abutting sidewalls of said semiconductor oxide containing gate dielectric portion and said doped semiconductor portion.

2. The semiconductor structure of claim **1**, wherein said high-k material portion further includes a chemical oxide portion vertically abutting said high-k material portion and said semiconductor substrate and comprising an oxide of a semiconductor material of said semiconductor substrate.

3. The semiconductor structure of claim **1**, wherein said oxygen-impermeable dielectric spacer has an L-shaped vertical cross-sectional area and vertically abuts said semiconductor substrate.

4. The semiconductor structure of claim **1**, further comprising another low-k gate spacer abutting said oxygen-impermeable dielectric spacer.

5. The semiconductor structure of claim **1**, wherein said oxygen-impermeable dielectric spacer comprises silicon nitride.

6. The semiconductor structure of claim **1**, wherein said low-k gate spacer comprises silicon oxide.

7. The semiconductor structure of claim **1**, wherein said low-k gate spacer comprises a low-k dielectric material having a dielectric constant less than 2.8.

8. The semiconductor structure of claim **1**, wherein said high-k material portion comprises one of HfO_2, ZrO_2, La_2O_3, Al_2O_3, TiO_2, $SrTiO_3$, $LaAlO_3$, Y_2O_3, HfO_xN_y, ZrO_xN_y, $La_2O_xN_y$, $Al_2O_xN_y$, TiO_xN_y, $SrTiO_xN_y$, $LaAlO_xN_y$, $Y_2O_xN_y$, a silicate thereof, and an alloy thereof, wherein each value of x is independently from about 0.5 to about 3 and each value of y is independently from 0 to about 2.

9. The semiconductor structure of claim **1**, wherein said metal gate portion comprises one of TiN, ZrN, HfN, VN, NbN, TaN, WN, TiAlN, TaCN, W, Ta, Ti, other conductive refractory metal nitrides, and an alloy thereof.

10. The semiconductor structure of claim **1**, wherein said high-k material metal gate structure further includes a second doped semiconductor portion comprising a doped semiconductor and vertically abutting said metal gate portion.

11. The semiconductor structure of claim **10**, wherein said semiconductor gate structure further includes a third doped semiconductor portion comprising said doped semiconductor and vertically abutting said doped semiconductor portion.

12. The semiconductor structure of claim **11**, wherein said third doped semiconductor portion and said doped semiconductor portion comprise different materials.

13. A method of forming a semiconductor structure comprising:

forming a first gate structure and a second gate structure on a semiconductor substrate, wherein said first gate structure includes a high dielectric constant (high-k) material portion having a dielectric constant greater than 8.0, and wherein said second gate structure includes a semiconductor oxide containing gate dielectric portion having a dielectric constant less than 8.0;

forming an oxygen-impermeable dielectric layer over said first gate structure and said second gate structure; and

removing a first portion of said oxygen-impermeable dielectric layer over said second gate structure, while protecting a second portion said oxygen-impermeable dielectric layer over said first gate structure.

14. The method of claim **13**, further comprising forming a low-k spacer having a dielectric constant less than 4.0 directly on sidewalls of said second gate stack and said second portion of said oxygen-impermeable dielectric layer.

15. The method of claim **14**, further comprising forming another low-k spacer having a dielectric constant less than 4.0 directly on sidewalls of said oxygen-impermeable dielectric layer over said first gate structure.

16. The method of claim **14**, further comprising etching said second portion of said oxygen-impermeable dielectric layer to form an oxygen-impermeable dielectric spacer.

17. The method of claim **16**, wherein said oxygen-impermeable dielectric spacer comprises silicon nitride and has an L-shaped cross-sectional area.

18. The method of claim **13**, wherein said first gate structure further includes a metal gate portion comprising a metal and vertically abutting said high-k material portion, and wherein said second gate structure further includes a first doped semiconductor portion comprising a doped semiconductor material and vertically abutting said semiconductor oxide containing gate dielectric portion.

19. The method of claim **18**, wherein said first gate structure further includes a chemical oxide portion vertically abutting said high-k material portion and said semiconductor substrate and comprising an oxide of a semiconductor material of said semiconductor substrate.

20. The method of claim **18**, further comprising:

forming a second doped semiconductor portion directly on said metal gate portion; and

forming a third doped semiconductor portion directly on said first doped semiconductor material portion, wherein said second doped semiconductor portion and said third doped semiconductor portion have an identical composition.

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